Delay-Line Sharing Based: A New 600-MHz 16-bit Resolution CMOS DPWM Circuit

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Abstract- This paper presents a new circuit design for digital pulse-width modulators (DPWM). In this paper, we improve the structure of hybrid DPWM by utilization of the separation of MSB/LSB group. In addition, a delay line element is shared by MSB/LSB group to reduce the power consumption. The new DPWM prototype circuit operates at 600 MHz clock frequency and has 1.1-mW power consumption. An experimental chip is fabricating by using a standard 0.18 micron CMOS process. The layout area is 461 um × 370 um. Post-layout simulation shows the new DPWM with advantages of smaller chip area and low power consumption especially for PWM with high resolution requirement.

Keywords: Digital Pulse-Width Modulators (DPWM), Pulse-Width Modulation, PWM.

1. Introduction

According to different signal modulations, analog pulse modulation system can be classified as Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), and Pulse Width Modulation (PWM). Based on the signal level, PAM modulates the amplitude of data pulses. However, the modulated data in a communication system are easily interference by noise disturbance, which leads to signal distortion. The method of PPM modulates data pulses with different phases according to the transmitted signal. The PPM demodulation in the received side, however, the hardware is not easy to realize. As a result, the cost of PPM realization is higher than PAM and PPM modulations. PWM modulates the pulse stream with various pulse's width according to signal level. PWM circuit has many advantages including of high performance, high anti-noise capability, and a wide range of applications.

Fig. 1 shows a conceptual block diagram of an analog PWM [2]. An analog input signal is compared with a given carrier to provide amplitude to time domain conversion. The output of carrier generator in general is a linear ramp waveform like as saw-tooth wave. The architecture is with advantages of simple circuit architecture and easy realization. Unfortunately, the performance of the architecture suffers higher sensitivity in temperature, process variation, and noise, etc. Based on the drawbacks and IC technology improvement, it seems to be a good selection to apply digital techniques to modulate data pulse width. An example of digital PWM architecture is shown in Fig. 2 [2]. The function of time quantizer, instead of the analog carrier generator shown in Fig. 1, which quantize time scale into a number of discrete time slots of length ***td***. A specific time slot is selected by the digital control input word ***d[n]***. The digital modulation has the advantages of a low-cost, low sensitivity, and low power. Observations from recent years, the digital modulation techniques are already widely used in electrical, electronic and other application fields. In the paper, we propose a new digital PWM circuit with advantages of sharing of delay elements to achieve small chip area and simpler circuit design.

The organization of the paper is described as follows. Section 2 briefly review various realized techniques for digital PWM circuits. Section 3 proposes the new digital PWM (DPWM) circuit. Section 4 shows the simulation results. Finally, conclusions of the paper are given in Section 5.

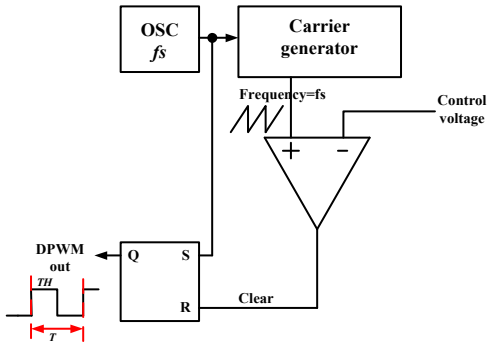

Fig. 1. Conceptual block diagram of analog PWM.

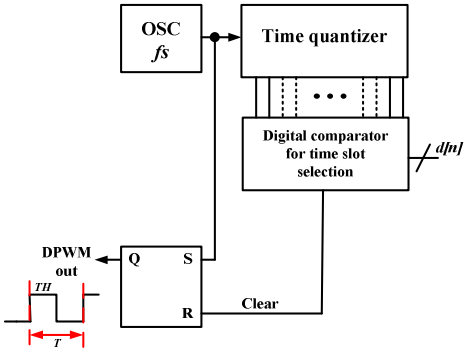

Fig. 2. Conceptual block diagram of digital PWM.

2. Previous Works of DPWM Architectures

In this section, we explore various techniques in the open literature for DPWM realization. The modulation techniques are divided into the following categories.

(1) DPWM Type I – Counter type:

Fig. 3 is block diagram for the counter method [3]. The method is based on a zero detection of a presetting counter count down operation. It needs two different clocks *fsw* and *fclk*. For this operation, a higher frequency *fclk* is required when the high resolution is needed. This method is with appropriate chip area, but it suffers from relatively high power consumption.

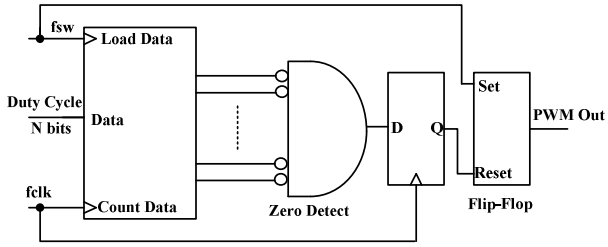

Fig. 3. Type I: counter type.

(2) DPWM Type II – Delay line:

Fig. 4 shows a block diagram for the delay line method [3]. The counter function shown in Fig. 3 is replaced by a serial of delay-line element. The architecture can relieve the problem of high power consumption. However, if DPWM *n*-bit resolution (pulse width modulated by 2^n states) is requirement, a delay line with length of 2^n stage is needed. The chip area will be greatly increased.

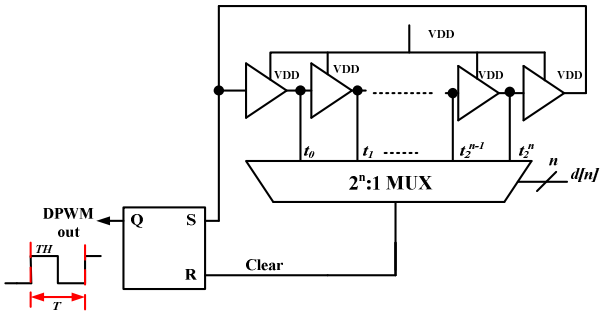

Fig. 4. Type II: Tapped delay line type.

(3) DPWM Type III – Hybrid DPWM:

Fig. 5 shows a hybrid DPWM architecture, which is combination of count and delay line types methods [1]. In 2003, the method was proposed by B. J. Patella, trying to achieve an optimization in the chip area and power consumption. The architecture will also suffer from larger chip area when high resolution is required.

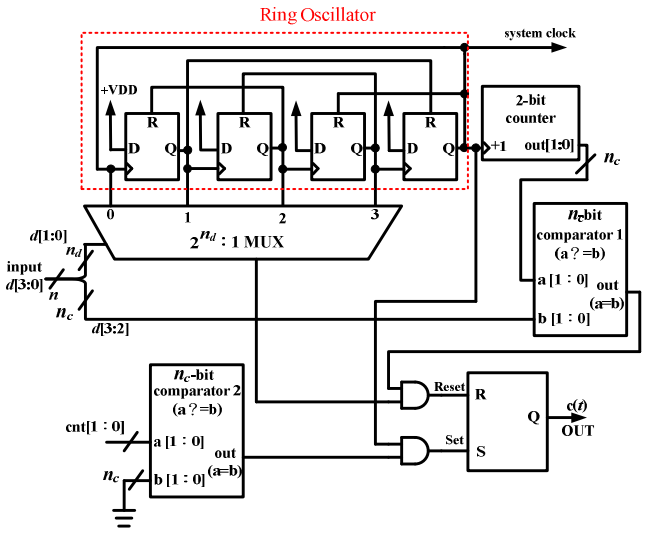

Fig. 5. Type III: Hybrid DPWM

(4) DPWM Type IV – Σ-ΔDPWM [4]:

This technique was proposed in the 1960s. The conceptual diagram is shown in Fig. 6. In recent years, it has begun more popular for communication and oversampling analog-to-digital converter. For high resolution PWM, the method is more accurate than others at the expenses of high complexity and high cost.

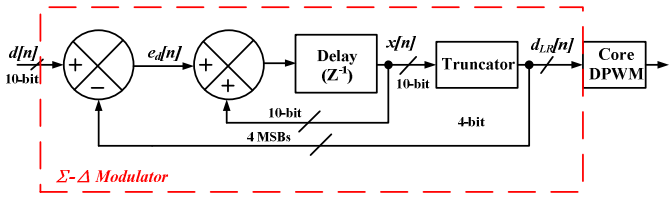

Fig. 6. Type IV: Σ - Δ DPWM

Although today Hybrid DPWM and Σ-Δ DPWM techniques are often apply to realize PWM circuit, these methodologies have drawbacks of high cost and high complexity. In this study, based on Hybrid DPWM architecture, we propose a new design to simplify the complexity of circuit. In addition, we utilize the common delay line elements to share between two MSB and LSB control parts. As a result, chip area and power consumption are improved.

3. Proposed DPWM Architectures

When conventional hybrid DPWM architecture operates in high-resolution requirement, the number of delay-line element increases in proportional to resolution bit *n*. Table 1 summarizes the number of required elements under various resolution bit *n*. For example, 16 bit resolution, the conventional architecture needs 256 delay elements while our proposed architecture only needs 128 delay elements.

Table 1. The specification of hybrid DPWM.

Bit *n*	no. of MUX	no. of counter	no. of delay line element
4	4×1	2	4
8	8×1	4	16
16	16×1	8	256

Fig. 7. The duty cycle of 4-bit DPWM.

Figure 7 describes an example for 4-bit PWM operation. In this example, 4-bit resolution allows 16 modulated statuses, pulse width ranges from 0/16, 1/16, 2/16, …, to 15/16. In Fig. 7, if we set the bits S3, S2, S1, and S0 as logic 1, 0, 1, and 0, respectively; that is,

$$1\times0 + 2\times1 + 4\times0 + 8\times1 = 10 \quad (1)$$

The circuit puts out at tenth status (9/16). In Fig. 8, the innovation of the paper is that the 4-bit number is divided into two parts: MSB and LSB groups. The bit number of MSB is amplified by weighted 4. Then the MSB value plus the LSB value also equals the result of (1). The procedure is described as

$$\text{the value of LSB group} = 1\times0 + 2\times1 = 2, \quad (2)$$
$$\text{the value of MSB group} = (1\times0 + 2\times1)\times4 = 8, \quad (3)$$
$$\text{MSB} + \text{LSB} = 8 + 2 = 10. \quad (4)$$

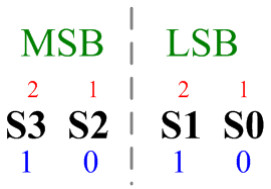

Fig. 8. The resolution bit is divided as MSB and LSB.

A new proposed hybrid DPWM composed of delay line, 2-bit DPWMFDC block, and MSB/LSB combination circuit shows in Figure 9. DPWMFDC block is composed by a 2-bit DPWM succeeding with frequency divider circuit. Delay line with reset function is realized by two-stage D flip-flop. The function of delay line is shared between two 2-bit DPWMFDC. Therefore, the chip area and power consumption of the proposed architecture are smaller than the traditional DPWM.

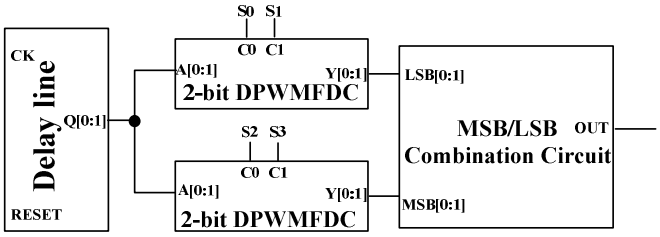

Fig. 9. Architecture of 4-bit new hybrid DPWM.

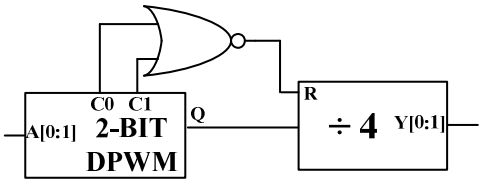

Fig. 10. 2-bit DPWMFDC**.**

Figure 10 shows the function blocks of the 2-bit DPWMFDC, in which including the 2-bit DPWM circuit, NOR gate, and a dvided-by-4 circuit. The PWM control of the 2-bit DPWM is set by C0 and C1. As C0 and C1 are set as "00", the divided-by-4 function is reset. C0 and C1 are set as range of "01"-"11", the frequency of signal Q is divided by 4 to create some proper time intervals. Figure 11 shows the circuit design for 2-bit DPWM [5].

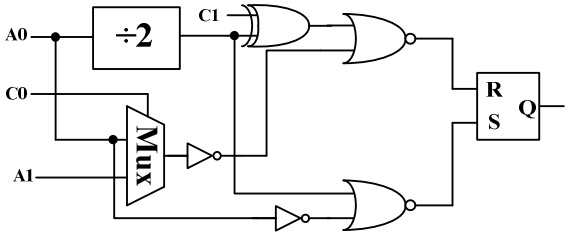

Fig. 11. Circuit design for 2-bit DPWM.

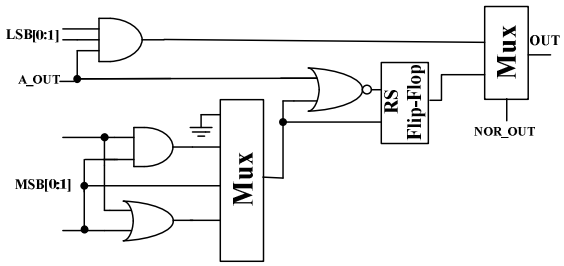

Fig. 12. MSB/LSB combination circuit.

Figure 12 shows the MSB/LSB combination circuit. Based on the circuit, either the output of 2-bit DPWMFDC (LSB) or the output of 2-bit DPWMFDC (MSB) will be selected by controlling bits S0-S3 and MSB/LSB combination circuit. Hence, the PWM modulated outputs 0/16 to 15/16 will be arrived.

4. Simulation Results

The HSPICE simulations have been performed on these circuits based on the TSMC 0.18 μm 1P6M mixed-mode process technology. Post-layout simulation waveforms for duty cycles 0/16, 8/16 (50 %) and 15/16 (93.75%) of the novel hybrid DPWM are shown in Fig. 13, respectively. Layout of the chip implementation of the novel hybrid DPWM is shown in Fig. 14. The active area is 0.461 mm × 0.37 mm.

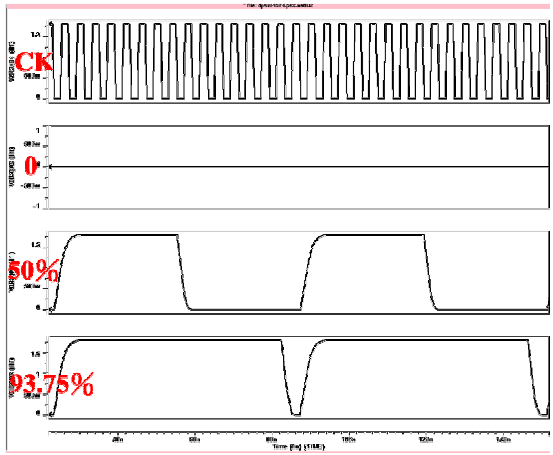

Fig. 13. Post-layout simulation of the proposed DPWM.

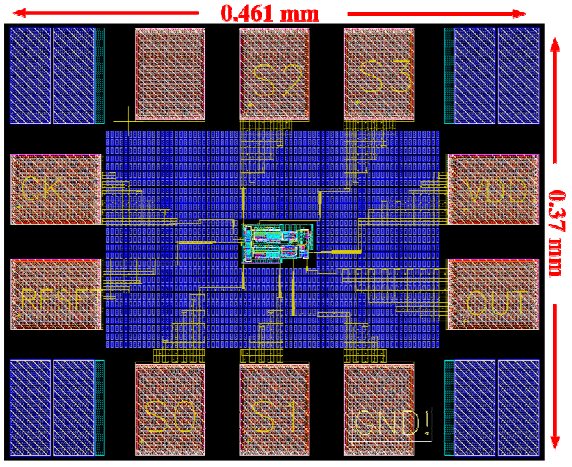

Fig. 14. Layout of the proposed hybrid DPWM.

5. Conclusions

This paper presents a technique survey and a design of the novel hybrid DPWM architecture with advantage of low-power consumption. Theoretical and simulation indicated that the designed DPWM can successfully 600 MHz clock frequency in 0.18-μm CMOS process, which satisfying 4-bit resolution requirement. The new hybrid DPWM chip area is 0.461mm×0.37mm and power consumption is 1.1mW.

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References

[1] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[2] A. Syed, E. Ahmed, D.Maksimovic, and E. Alarcon, "Digital pulse width modulator architectures," in *Proc. IEEE PESC Conf.*, 2004, pp. 4689– 4695

[3] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," in *Proc. IEEE PESC Conf.*, 1997, pp. 21–27.

[4] Z. Lukic, N. Rahman, and A. Prodic, "Multi Σ − Δ PWM digital controller IC for DC–DC converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1693– 1707, Sep. 2007

[5] Y.C. Hung and K.C. Tsai, "High-Stability LED PWM Driver Core with 16 Levels Capability," *Proceedings of the Fourth Intelligent Living Technology Conference (2009) 828-831.*

[6] Y.C. Hung and K.C. Tsai, "High-Frequency 700MHz LED PWM Driver Core with 16 Levels Capability," *Conference on Innovative Applications of System Prototyping and Circuit Design* (2009) 368-371.

[7] W. Gu-Yeon and M. Horowitz, "A low power switching power supply for self-clocked systems," *in Proc. Int. Symp. Low Power Electron. Des.*, 1996, pp. 313–317.

[8] E. O'Malley and K. Rinne, "A programmable digital pulse width modulator providing versatile pulse patterns and supporting switching frequencies beyond 15 MHz," in *Proc. IEEE APEC Conf.*, 2004, pp. 53–59.

[9] V. Yousefzadeh, T. Takayama, and D. Maksimovic, "Hybrid DPWM with digital delay-locked loop," in *Proc. IEEE Comput. Power Electron.*, 2006, pp. 142–148